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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,252	06/27/2003	Anthony L. Priborsky	STL11196	8554

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EXAMINER
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FLOURNOY, HORACE L

ART UNIT	PAPER NUMBER
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2189

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/608,252	<b>Applicant(s)</b> PRIBORSKY ET AL.	
	<b>Examiner</b> Horace L. Flournoy	<b>Art Unit</b> 2189	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 6 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 December 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 16 and 17 is/are allowed.
- 6) ☒ Claim(s) 1,3,5,7,9-11 and 18-24 is/are rejected.
- 7) ☒ Claim(s) 2,4,6,8 and 12-15 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Response to Amendment*

This Office action has been issued in response to amendment filed 15 December 2005. Claims 1-24 are pending. Applicant's arguments have been carefully and respectfully considered and are persuasive. New grounds for rejection have been set forth as a result of the instant arguments. Accordingly, this action has been made NON-FINAL.

The instant application having Application No. **10/803,289** has a total of 24 claims pending in the application; there are 3 independent claims and 21 dependent claims, all of which are ready for examination by the examiner.

## INFORMATION CONCERNING OATH/DECLARATION

### *Oath/Declaration*

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63**.

### *Specification*

The examiner has noted the amendment to the **abstract** of the disclosure. The objection in the previous Office Action is herewith withdrawn.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere CO.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

**Claims 1, 3, 5, 7, 9, 10, 11, and 18-24** are rejected under 35 U.S.C. 103(a) as being obvious over Larson (U.S. Patent no. 6,321,233, hereafter referred to as Larson) in view of Chan et al. (US Patent No. 5,822,772 hereafter referred to as Chan).

With respect to independent **claim 1**,

*"A method comprising steps of: (a) assigning a unique tag for each of several disc access commands; [Chan discloses in column 2, lines 7-10, "...each transaction is attached with a tag and the transactions on the bus are recognized by their tags but not by their orders." See FIG. 4] and (b)*

*designating which of a plurality of queue execution modes to use for a selected one of the disc access commands based on the selected command's tag."* **[is disclosed in Larson in column 9, lines 64-67 and column 10, lines 1-5]**

Larson does not expressly teach the limitations cited supra by Chan.

Larson and Chan are analogous art because they are from the same field of endeavor that being controlling memory access commands.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate assigning a unique tag to several data access commands with using these tags to designate a particular queue execution mode to arrive at the amended claim 1.

The motivation for doing so would have been obvious based on the teaching of Larson at column 2, lines 27-36.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Larson and Chan before him/her to combine Chan and Larson for the benefit of assigning a unique tag to several data access commands and using these tags to designate a particular queue execution modes to arrive at claim 1.

With respect to **claim 3**,

"The method of claim 1, further comprising a step of establishing a contiguous range of tags that includes the selected command's tag, the contiguous range corresponding to the mode to be designated in the designating step (b)" is disclosed in column 9, lines 41-44.

The examiner interprets claim 3 as meaning to order (or establish) the tags in a contiguous range (including selected command's tag) by tag type or queue execution mode.

Larson discloses in column 9, lines 41-44, "...a read age tag buffer operable to store the age tags assigned to each of the read requests; and a write age tag buffer operable to store the age tags assigned to each of the write requests." As such, Larson is ordering the tags in a contiguous range (in this case buffer). The "read age tag buffer" and the "write age tag buffer" are each interpreted as a "mode" which corresponds to a read request and a write request, respectively.

With respect to **claim 5**,

"The method of claim 1, further comprising steps of: (c) associating one of the queue execution modes with a first queue..." is disclosed in column 9, lines 53-55. The examiner interprets this limitation as simply associating one group of queue execution modes to a first queue. Larson discloses in column 9, lines 53-55 "...a read queue operable to receive and store a plurality of pending read requests..." Larson is associating a particular queue execution mode (in this case 'read') with a first or distinct queue.

With respect to claim 5(d), "associating another of the queue execution modes with a second queue..." is disclosed in column 9, lines 53-55. The examiner interprets this limitation as simply associating another group of queue execution modes to a second (or distinct from the first) queue. Larson discloses

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in column 9, lines 53-55 "...a write queue operable to receive and store a plurality of pending write requests..." Larson is associating a particular queue execution mode (in this case 'write') with a second or another distinct queue.

With respect to claim 5(e), "performing an operation that affects at least one command in the first queue without affecting a command that is in the second queue" is disclosed in column 7, lines 18-19. The examiner interprets this limitation as to perform an operation in one (first) queue without affecting the other (second) queue. Larson teaches in column 7 (lines 18,19) that the write requests and the read requests are separated into separate queues. Larson goes on to disclose in column 7, lines 26-29, FIGS. 5-8, element 64 "Ordering of write requests relative to one another is accomplished by the inherent ordering of the write request FIFO, as is ordering of the various read requests relative to one another in the read request FIFO." These teachings demonstrate that there are operations done in the read request queue that do not affect the write request queue, since they are both ordered in their respective queues. To further clarify, "ordering" must be done on at least one command.

**With respect to claim 7,**

"The method of claim 1, further comprising a step (c) of redefining a queue execution mode that is associated with at least one tag while the at least one tag is not assigned to any disc access command" is disclosed in column 2, lines 58-64.

Claim 7 is interpreted as redefining (or modifying) a queue execution mode (or tag type for a particular queue) that is associated with at least one tag while that same tag is not yet assigned to any disc access commands (examined interpretations in parenthesis).

Larson anticipates this claim in column 2, lines 58-64. Larson, in this reference, also discloses "decrementing not-zero write tags," which is also interpreted as modifying a queue execution mode.

With respect to **claim 9**,

"The method of claim 1, further comprising a step (c) of using at least one of the queue execution modes to transfer video data through a transducer adjacent to a data storage disc" is disclosed in column 1, lines 27-28, column 3, lines 60-61, and column 4, lines 27-31. The examiner interprets claim 9 as designating one of the queue execution modes to transfer video data through a transducer adjacent to a data storage disc.

Larson discloses in column 1, lines 57-59, FIG. 1 elements 206 and 214, "using at least one of the queue execution modes to transfer video data..." by stating "The AGP interface circuitry includes a request queue that stores a plurality of memory access requests from the graphics controller for subsequent service by the memory controller." Larson also discloses the usage of "a data storage device, such as a disk drive..."(column 3, lines 60, 61). The use of a transducer (adjacent to a data storage disc) in a data storage disc is inherent. To clarify, Larson discloses in column 4, lines 26-31, "Those skilled in the art will understand that the AGP interface, the AGP bus, and associated graphics



circuitry represent one possible example of circuitry for pipelining data transfer requests to the system memory.” As cited above, the particular queue execution mode is interpreted as being an element of the AGP interface circuitry (request queue), while video data is transferred to a system memory (i.e. data storage disc) through a transducer.

With respect to **claims 10 and 11**,

“The method of claim 1(claim 9), in which the designating step (b) includes a step (b1) of determining whether to use a sequential delivery mode for the selected disc access command” is disclosed in column 2, lines 27-31, FIG. 1, element 214. The examiner interprets claims 10 and 11 as to determine whether to use a sequential delivery mode (i.e. FIFO) for a selected disc access command. To clarify, “sequential delivery mode” can be used to describe a mode, which employs a First-In, First-Out (FIFO) delivery. Larson discloses “Allowing write operations to pass read operations means that the request queue does not function strictly as a first-in first-out (FIFO) buffer...” Next, Larson discloses in column 2, lines 46-50, “The read and write age tags may themselves be stored in separate read and write age queues or FIFOs included within the pipeline controller circuitry.” In other words Larson teaches a method in which read and write operations or read and write age tags (disc access commands) can be (determining whether to) used in a sequential delivery mode (FIFO). Larson clearly anticipates claim 11 through the aforementioned teachings.

With respect to independent **claim 18**,

"An electromechanical device comprising: one or more data storage disc(s) **[disclosed in Larson column 3, lines 60-61, FIG. 2 element 42. Larson discloses the usage of "a data storage device, such as a disk drive..."]** a memory configured to hold several pending commands for accessing the disc(s), each of the commands having a unique tag; and a controller configured to determine which of a plurality of queue execution modes to use for a selected one of the pending disc access commands based on the selected command's tag" **[Chan discloses in column 2, lines 7-10, "...each transaction is attached with a tag and the transactions on the bus are recognized by their tags but not by their orders." See FIG. 4 of Chan]**

Larson and Chan are analogous art because they are from the same field of endeavor that being controlling memory access commands.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate assigning a unique tag to several data access commands with using these tags to designate a particular queue execution mode to arrive at the amended claim 1.

The motivation for doing so would have been obvious based on the teaching of Larson at column 2, lines 27-36.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Larson and Chan before him/her to combine Chan and Larson for the benefit of assigning a unique tag to several data access commands and using these tags to designate a particular queue execution modes to arrive at claim 1.

**Claim 19** is rejected under 35 U.S.C. 103(a) as being obvious over Larson in view of Chan in further view of Snyder, II (US Patent No. 6,189,083 hereafter referred to as Snyder).

Larson teaches claim 18 (upon which claim 19 is dependent).

Larson, however, does not disclose expressly a "memory configured to hold the tag as a binary value no larger than one byte." Although Larson teaches the usage of a memory configured to hold the tag (Larson column 9, lines 40-41), it does not include reference as to the size (and format) of the tag value, specifically, "a binary value no larger than one byte," as stated in claim 19.

Snyder discloses in column 5, lines 20-21 "a cache sub-system having two tag sub-stores, each including a plurality of four-bit tags."

Larson and Snyder are analogous art because they are from the same field of endeavor, that being ordering or controlling memory commands.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to simply include a specification that entails a binary tag value, which is not larger than one byte.

The motivation for doing so would have been obvious based on the following reference: "The associated age tag values are 0, because there were no previously received and pending requests in the write queue." (Larson column 6; lines 22-23; FIGS. 5-9) Larson goes on to teach tag values of "2" or "3" (Larson column 6; line 31 and line 34; FIGS. 5-9). It would be obvious to someone of ordinary skill in the art to associate value 0 with binary value "0000" or "00", etc, and likewise associating 2 with binary value "0010."

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Larson and Snyder before him/her for the benefit of having a memory, which is configured to hold the tag (already in integer form) as a binary value (e.g. "0010") no larger than one byte to obtain the invention as specified in claim 19.

**Claim 20** is rejected under 35 U.S.C. 103(a) as being obvious over Larson in view of Chan in further view of Ng (U.S. Patent No. 5,341,351 hereafter referred to as Ng).

Larson teaches (as previously discussed) claim 18 (upon which claim 20 is dependent).

Larson does not disclose expressly "an actuator having a nominal seek time longer than 1 millisecond."

Ng discloses, "a dual actuator DASD such as shown in FIG. 1 has an average seek time of 10 milliseconds..." (Ng column 6, lines 34-36, FIG. 1)

Larson and Ng are analogous art because they are from the same field of endeavor, that being ordering or controlling memory commands.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include an actuator, of which is present in many (electromechanical) "data storage devices" (Larson column 3, lines 60-61, figure 2, element 42), which has a nominal seek time longer than 1 millisecond onto a data storage disc (device).

The motivation for doing so would have been obvious since Ng discloses, "...the seek times of such a movable arm or actuator access are in the order of milliseconds (e.g.  $25 \cdot 10^{-3}$ ) rather than microseconds (e.g.  $5 \cdot 10^{-6}$ ). The actual

convergence of an actuator and transducer on any selected track utilizes feedback involving minimizing the error..."(column 1, lines 60-65). To clarify "selected track" Ng also discloses [in reference to moving magnetic storage], "Data in the form of patterns of magnetic spots are recorded along one or more tracks following a predetermined format" (column 1, lines 26-29). As discussed supra, the use of a transducer with a DASD is inherent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Larson and Ng before him/her for the benefit of having a data storage disc (with limitations of claim 18) further including an actuator (with nominal seek time longer than 1 millisecond) to obtain the invention as specified in claim 20.

**Claim 21** is rejected under 35 U.S.C. 103(a) as being obvious over Larson (U.S. Patent no. 6,321,233) in view of Chan in further view of Hoang et al. (U.S. Patent No. 6,026,469 hereafter referred to as Hoang), with MPCD offered as extrinsic evidence.

Larson teaches (as previously discussed) claim 18 (upon which claim 21 is dependent).

However, Larson does not disclose expressly "...the memory includes a multiple-bit state register configured to identify one or more other tags that are available for a future command."

Hoang discloses that "Firmware reads the state of register and uses this information to set registers in memory/cache bridge and controller for managing the 8 tag bit or 11 tag bit L2 cache module" (Hoang column 3; lines 41-44; FIG. 1, elements 16 and 9)

Larson and Hoang are analogous art because they are from the same field of endeavor, that being ordering or controlling memory commands.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to configure a multiple-bit state register to identify (or manage) future (or stored) commands. By definition, a register is a set of bits of high-speed memory... (Microsoft Computer Dictionary, 5<sup>th</sup> Ed., page 445) To further clarify, Hoang's register discloses identifying (or managing) multiple-bits (8 bit tag or 11 bit tag).

The motivation for doing so would have been obvious since Hoang discloses, "...there has arisen the need for personal computers or workstations have the capability of discerning whether an L2 module that is detected as being present is either the 8 tag bit or 11 tag bit variety" (column 1, lines 49-54). The "L2 module" is a form of cache memory.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Larson and Hoang before him/her for the benefit of having a state register (multiple bit and within memory) that identifies (or manages) one or more tags that are available for a future (or stored) command to obtain the invention as specified in claim 21.

**Claim 22** is rejected under 35 U.S.C. 103(a) as being obvious over Larson in view of Chan in further view of Zuravleff et al. (U.S. Patent No. 5,737,547 hereafter referred to as Zuravleff).

Larson discloses (as previously discussed) claim 18 (upon which claim 22 is dependent

Larson does not disclose expressly "...the queue execution modes include a higher priority mode associated with a first queue and a lower-priority mode associated with a second queue."

Zuravleff discloses, "Each of these pending sub-queues is assigned a unique priority level. In the simplest implementation of this multiple-priority version of the non-blocking load buffer, illustrated in FIG. 9(b), there are two pending sub-queues 214<sub>0</sub> and 214<sub>1</sub> for a peripheral device with sub-queue 214<sub>0</sub> being assigned a high priority and sub-queue 214<sub>1</sub> assigned low priority" (column 10; lines 50-56; FIG. 9 (b) elements 214<sub>0</sub> and 214<sub>1</sub>). As apparent from the above-cited FIG. 9(b), "sub-queues" are, in fact, separate, functional queues. Zuravleff further discloses, "the priority level may be identified by adding a priority tag to the memory transaction. This priority tag is used to channel the memory transaction into the pending sub-queue with matching priority level..." (column 11, lines 10-13).

Larson and Zuravleff are analogous art because they are from the same field of endeavor, that being ordering or controlling memory commands.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to assign high priority to a read queue and a low priority to a write queue, or vice versa.

The motivation for doing so would have been obvious since Larson does disclose, "High priority requests are used very infrequently, such as when a request needs immediate processing. Low priority requests represent the large majority of memory access requests..." (column 2, lines 5-9). ). Larson also teaches, "the request queue may include both high priority and low priority

requests, which have separate priority and ordering rules.” (column 2; lines 3-5; FIG. 1, element 214) Since high priority requests (or commands) and low priority requests (or commands) “have separate priority and ordering rules” it would be natural and obvious to split them into separate queues. Furthermore, Zuravleff teaches, (column 11, lines 40-53) “Figure 3 (b) illustrates memory latency for the multiple-priority non-blocking load buffer. In this example, processor B's memory transactions are assigned a higher priority than processor A's memory transactions. Therefore, transaction B2 is delivered to the memory before transactions A2 and A3 even though the request to begin transaction B2 arrived at the non-blocking load buffer after requests A2 and A3. As a result, the latency for transaction B2,  $t_{B2}$  is less in Figure 3(b) than  $t_{B2}$  in Figure 3(a), which illustrates a non-blocking load buffer that does not offer the benefit of multiple-priority scheduling. Using the multiple-priority version of the non-blocking load buffer, Processor B spends less time stalled waiting for transaction B2 to complete as illustrated by the comparison in Figures 3(a) and 3(b).”

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Larson and Zuravleff before him/her for the benefit of having tags that identify commands (read or write) to either a high priority queue or low priority queue (queue execution mode) to obtain the invention as specified in claim 22.

With respect to **claim 23**,



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Larson teaches in column 2, lines 46-50, "The read and write age tags (plural, i.e. more than zero) may themselves be stored in separate read and write age queues or FIFOs included within the pipeline controller circuitry."

The examiner interpreted this claim to mean a first queue (or mode) with more than 0 tags stored and a second queue (or mode) with more than 0 tags stored in it.

**Claim 24** is rejected under 35 U.S.C. 103(a) as being obvious over Larson in view of Chan in further view of Morrow (U.S. PG Pub No. US 2003/0046472 hereafter referred to as Morrow).

Larson discloses (as previously discussed) claim 18 (upon which claim 24 is dependent).

Larson does not disclose expressly that, "...the controller is operatively coupled to communicate with a host through a serial ATA bus."

Morrow discloses, "...the enhanced converter/controller device for the purposes of offloading instructions to the platform central processing unit. The intermediate off-loading instructions electrical interface typically comprises a standard interface connection, such as...Serial ATA...bus interface." (Morrow page 5; [0066]; FIG. 3, elements 74,82) Furthermore, FIG. 3 element 72 of Morrow teaches an "enhanced host system" to which the controller communicates.

Larson and Morrow are analogous art because they are from the same field of endeavor, that being ordering or controlling memory commands.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to define memory access (pending commands with tags) to communicate with a host over a serial ATA bus (widely used for disc controllers).

The motivation for doing so would have been obvious based on the following reference from Morrow: " [0066] The intermediate off-loading electrical interface 82 and intermediate protocol support logic 80 provides an additional interface, either logical or physical, to the enhanced converter/controller device 74, for purposes of offloading instructions to the platform central processing unit 18. The intermediate off-loading electrical interface 82 typically comprises a standard interface connection 82, such as...Serial ATA" (Morrow page 5; [0066]; FIG.1 elements 82, 80, 74, 18).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Larson and Morrow before him/her for the benefit of having a controller that communicates to a particular host through a serial ATA bus to obtain the invention as specified in claim 24.

**Allowable Subject Matter**

**Claims 2, 4, 6, 8, and 12-15** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

**Claims 16 and 17** are allowable.

The primary reasons for allowance of claim 16 in the instant application is the combination with the inclusion in these claims the limitation of **assigning a second standard queue tag to a third-received one of the commands while the first-and second-received commands are both still pending, the third-received command being a standard write command; assigning another tag to a fourth received one of the commands while the third received command is still pending.**

Claim 17 depends upon the instant claim, and is allowable for at least the reasons set forth supra with respect to same.

The prior art of record neither anticipates nor renders obvious the above-recited combination.

**:IMPORTANT NOTE:**

If the applicant should choose to rewrite the independent claims to include the limitations recited in claim 14, the applicant is encouraged to amend the **title of the invention** such that it is descriptive of the invention as claimed as required by sec. 606.01 of the MPEP. Furthermore, the **Summary of the Invention** and the **Abstract** should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of sec. 1302.01 of the MPEP.

As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See **37 C.F.R. § 1.111(b)** and **§ 707.07(a) of the M.P.E.P.**

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

### ***CONCLUSION***

**THIS ACTION IS MADE NON-FINAL.**

### **Direction of Future Correspondences**

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

**Important Note**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Horace L. Flournoy

Patent Examiner

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*Reginald G. Bragdon*  
REGINALD G. BRAGDON  
PRIMARY EXAMINER

Supervisory Patent Examiner

Technology Center 2100